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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|-----------------------|------------------|
| 10/696,918 | 10/30/2003 | Robert S. Vinson | GCSD-1157 (51231-DIV) | 8239 |

7590 06/03/2005

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EXAMINER

TRAN, THANH Y

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/696,918

Applicant(s)

VINSON ET AL.

Examiner

Thanh Y. Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 March 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10-18,28,30 and 38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10-18,28,30 and 38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 10/30/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Applicant's election with group I, claims 10-18, 28, 30 and 38 which was filed on 03/14/05 is acknowledged. However, applicant has not stated whether the election is with or without traverse. Therefore, it is treated as without traverse.

Further, since the examiner has distinctly pointed out three different groups with three different class/sub-class areas, the examiner does believe that there exists a serious burden to search all claims.

Drawings

1. The drawings are objected to because element "16b" as shown in figure 4 is used to disclose a sidewall of the decoupling capacitor 16, while in figure 3 "16b" is used to disclose for an adhesive underneath the decoupling capacitor 16. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not

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accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "14" and "31" in figure 4 have both been used to designate "IC" chip.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 11 is objected to because of the following informalities: the limitation "a plurality of decoupling capacitor assemblies mounted on said integrated circuit die" as recited in claim 11 is confusing because figure 2 only shows "a plurality of decoupling capacitor assemblies mounted on a substrate 12, not on the integrated circuit die". For the examining purpose, the examiner will assume that a plurality of decoupling capacitor assemblies mounted on the substrate for the above limitation. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 10,13-16, 18, 28, 30 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Spielberger et al (U.S. 6,005,778).

As to claim 10, Spielberger et al discloses in figure 6 an integrated circuit chip module comprising: a substrate (as indicated at 14 in figure 1, or 14b in figure 5); an integrated circuit die ("chip" 40c) mounted on the substrate and having die pads (which are connected to wire bonds 90 on chip 40c) and an exposed surface opposite from the substrate; a plurality of substrate bonding pads (18c, 19c) positioned on the substrate adjacent the integrated circuit die ("chip" 40c); and a decoupling capacitor assembly (comprising elements 82, "metal layer" 86, and 70) (col. 5, lines 8-9) mounted on the integrated circuit die ("chip" 40c), the decoupling capacitor assembly comprising a capacitor carrier ("spacer" 50b) (as indicated in figure 5) secured onto the exposed surface of the integrated circuit die ("chip" 40c), a decoupling capacitor (70) carried by the capacitor carrier; a thin film metallization layer ("metal layer" 86) (col. 5, lines 8-9) positioned on the capacitor carrier ("spacer" 50b) (as indicated in figure 5); and a conductive adhesive layer (90) (col. 5, lines 6-7) engaging the decoupling capacitor (70) and thin film metallization layer ("metal layer" 86) (col. 5, lines 8-9) and securing the decoupling capacitor (70) to the capacitor carrier ("spacer" 50b) (as indicated in figure 5); a wire bond extending from the thin film metallization layer ("metal layer" 86) (col. 5, lines 8-9) to a logic pin (a logic pin is a bonding pad on chip 40c) of the integrated circuit die ("chip" 40c) and from a logic pin to a substrate bonding pad (18c).

As to claim 13, Spielberg et al discloses in figure 6 an integrated circuit chip module further comprising: an adhesive (90) (col. 5, lines 6-7) securing the decoupling capacitor (70) to the capacitor carrier ("spacer" 50b) (as indicated in figure 5).

As to claim 14, Spielberg et al discloses in figure 6 an integrated circuit chip module further comprising: an adhesive ("electrically conductive adhesive") securing the decoupling capacitor assembly (spacer 50 as indicated in figure 4) to the integrated circuit die (40c or 40a in figure 4) (col. 4, lines 5-30).

As to claim 15, Spielberg et al discloses in figure 6 an integrated circuit chip module, wherein the capacitor carrier ("spacer" 50b) (as indicated in figure 5) is formed from an aluminum nitride substrate ("aluminum nitride") (col. 4, lines 5-16; and col. 6, lines 50-53).

As to claim 16, Spielberg et al discloses in figure 6 an integrated circuit chip module, wherein the aluminum nitride substrate ranges in thickness from about 5 mil to about 50 mil ("approximately 40 mils") (col. 2, lines 65-67).

As to claim 18, Spielberg et al discloses in figure 6 an integrated circuit chip module including: a bonding pad ("dielectric material layer" 84) (col. 4, line 66 – col. 5, line 3) on the thin film metallization layer ("thin metal layer or film" 86) for securing a wire bond.

As to claim 28, Spielberg et al discloses in figure 6 a decoupling capacitor assembly (comprising elements 82, "metal layer" 86, and 70) (col. 5, lines 8-9) used for decoupling integrated circuit die ("chip" 40c) comprising: a capacitor carrier ("spacer" 50b) (as indicated in figure 5) formed as an aluminum nitride substrate ("aluminum nitride") (col. 4, lines 5-16; and col. 6, lines 50-53) that is about 5 mil to about 50 mil thickness ("approximately 40 mils") (col. 2, lines 65-67); a decoupling capacitor (70) carried by the capacitor carrier ("spacer" 50b) (as

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indicated in figure 5); an adhesive (90) (col. 5, lines 6-7) securing the decoupling capacitor (70) to the capacitor carrier ("spacer" 50b) (as indicated in figure 5); and a thin film metallization layer ("metal layer" 86) (col. 5, lines 8-9) formed on the capacitor carrier ("spacer" 50b) (as indicated in figure 5), wherein the adhesive (90) comprises a conductive adhesive (col. 5, line 6) for conducting current between the capacitor and the capacitor carrier (see col. 5, line 6; and col. 4, lines 40-44).

As to claim 30, Spielberg et al discloses in figure 6 a decoupling capacitor assembly (comprising elements 82, "metal layer" 86, and 70) (col. 5, lines 8-9) used for decoupling integrated circuit die ("chip" 40c) further comprising: a bonding pad ("dielectric material layer" 84) (col. 4, line 66 – col. 5, line 3) positioned on said capacitor carrier ("spacer" 50b) (as indicated in figure 5) for connecting a wire bond thereto.

As to claim 38, Spielberg et al discloses in figure 6 an integrated circuit chip module comprising: a substrate (as indicated at 14 in figure 1, or 14b in figure 5); an integrated circuit die ("chip" 40c) mounted on the substrate and having die pads (which are connected to wire bonds 90 on chip 40c) and an exposed surface opposite from the substrate; a plurality of substrate bonding pads (18c, 19c) positioned on the substrate adjacent the integrated circuit die ("chip" 40c); and a decoupling capacitor assembly (comprising elements 82, "metal layer" 86, and 70) (col. 5, lines 8-9) mounted on each integrated circuit die ("chip" 40c), the decoupling capacitor assembly comprising a capacitor carrier ("spacer" 50b) (as indicated in figure 5) secured onto the exposed surface of the integrated circuit die ("chip" 40c), and a decoupling capacitor (70) carried by the capacitor carrier ("spacer" 50b) (as indicated in figure 5); a wire bond extending from the decoupling capacitor assembly (comprising elements 82, "metal layer"

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86, and 70) (col. 5, lines 8-9) to a die pad (a die pad is a pad on chip 40c) and from a die pad to a substrate bonding pad (18c); and a wire bond extending from the capacitor carrier ("spacer" 50b) (as indicated in figure 5) to a logic pin (a logic pin is a pad on chip 40c) of said integrated circuit die (chip 40c).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Spielberg et al (U.S. 6,005,778) in view of Liu et al (U.S. 6,429,536).

As to claim 17, Spielberg et al does not disclose a wire bond extends from the decoupling capacitor to a logic pin of integrated circuit die.

Liu et al discloses in figures 3-4 a wire bond (140) extends from the decoupling capacitor (120) to a logic pin ("bonding pad" 110a) of integrated circuit die ("chip" 110) (see col. 3, line 50 - col. 4, line 10). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the integrated circuit chip module of Spielberg et al by having a wire bond extends from the decoupling capacitor to a logic pin of integrated circuit die as taught by Liu et al for obtaining a stable wire loop shape with a high shape-retaining strength thereby preventing the bonding wire from contacting the surface-mountable device and causing a short circuit (see col. 1, line 62 - col. 2, line 5; and col. 3, line 50 - col. 4, line 10 in Liu et al).

8. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spielberger et al (U.S. 6,005,778) in view of Watanable et al (U.S. 6,873,035).

Spielberger et al does not disclose a plurality decoupling capacitor assemblies mounted on the substrate.

Watanable et al discloses in figure 12 a plurality decoupling capacitor assemblies (comprising elements 6 and 4A; and elements 6 & 4B) mounted on the substrate (2). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the integrated circuit chip module of Spielberger et al by having a plurality decoupling capacitor assemblies mounted on the substrate as taught by Watanable et al for reducing the power noises due to the chip module or improving the power source and ground characteristics at low cost.

As to claim 12, Spielberger et al discloses in figure 6 an integrated circuit chip module, wherein the plurality of decoupling capacitors (70) are mounted in series along the integrated circuit die (40c).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ball (U.S. 6,407,456) discloses multi-chip device utilizing a flip chip and wire bond assembly.

Her et al (U.S. 6,650,009) discloses structure of a multi chip module having stacked chips.

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Akram (U.S. 6,441,483) discloses die stacking scheme.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT



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